Patent claims

1. A method for producing vertically integratable circuits, characterized in that electrically conductive contacts for vertical integration are produced using method steps serving to produce the integratable circuits themselves.

2. A method according to claim 1, comprising the steps:

a) producing an insulation at the places of the contacts for vertical integration from the front side of a substrate bearing the vertically integratable circuits,

b) producing a gap within the insulations from the front side,

c) filling the gaps with an electroconductive material from the front side,

d) exposing the electroconductive material from the backside of the substrate bearing the vertically integratable circuits at the places of the contacts for vertical integration, and

e) applying an electroconductive material from the backside, in particular to the previously exposed electric material at the places of the contacts for vertical integration.

3. A method according to claim 2, characterized in that the substrate is thinned from the backside before exposure of the electroconductive material from the backside.

4. A method according to claim 3, characterized in that the substrate has a hidden insulating layer and thinning is performed as far as said insulating layer.

5. A method according to claim 3, characterized in that thinning is performed until the insulation produced for the contacts for vertical integration is reached.

6. A method according to any of claims 2 to 5, characterized in that the insulation produced in method step a) is produced during production of field oxide, with gaps being formed in the substrate that enclose substrate material that oxidizes completely during production of the field oxide.

7. A method according to any of claims 2 to 6, characterized in that the gaps produced in method step b) within the insulations and the filling of said gaps according to method step c) with an electroconductive material are performed during production of a metalization level with associated through holes.

8. A method according to any of claims 2 to 7, characterized in that the electroconductive material applied in method step e) is applied in a backside metalization.

9. A vertically integratable circuit having electrically conductive contacts for electrically conductive connection with further vertically integratable circuits, characterized in that the electrically conductive contacts used for vertical integration and associated insulations are produced during production of the vertically integratable circuit itself.

10. A vertically integratable circuit according to claim 9, characterized in that at least two vertically integratable circuits are connected, and their electrically conductive contacts for vertical integration are electrically connected with each other.